

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/626,475	WANG, BOW-YAW	
Examiner Helen Rossoshek		Art Unit 2825	Page 1 of 2	

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2002/0178424	11-2002	Gupta et al.	716/5
	B	US-6,745,160	06-2004	Ashar et al.	703/14
	C	US-6,484,134	11-2002	Hoskote, Yatin V.	703/14
	D	US-6,163,876	12-2000	Ashar et al.	716/5
	E	US-5,331,568	07-1994	Pixley, Carl	716/3
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Sheeran et al., "Checking Safety Properties Using Induction and a SAT-Solver", November 2000, In Proc. Conference on Formal Methods in Computer-Aided Design,
	V	Wedler et al., "Using RTL statespace information and state encoding for induction based property checking", 2003, Design, Automation and Test in Europe Conference and Exhibition, Pages:1156 - 1157
	W	Wedler et al., "Exploiting state encoding for invariant generation in induction-based property checking", 27-30 Jan. 2004, Desi Automation Conference, 2004. Proceedings of the ASP-DAC 2004. Asia and South Pacific , Pages:424 - 429
	X	Shende et al., "Synthesis of reversible logic circuits", June 2003, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 6, Pages:710 - 722

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<b>Notice of References Cited</b>		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/626,475	WANG, BOW-YAW	
Examiner		Art Unit	2825	Page 2 of 2
Helen Rossoshek				

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Prakash et al., "A high-performance architecture and BDD-based synthesis methodology for packet classification", June 2003, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 22 , Issue: 6, Pages:698 - 709
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.